UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
[illegible]

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
20/065,257	09/25/2002	Chih-Cheng Liu	NAUP0472USA	6305

7590 07/30/2003

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.	Applicant(s)
10/065,187	LIU ET AL
Examiner	**Art Unit**
Mai-Huong Tran	2818

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4)☐ Interview Summary (PTO-413) Paper No(s). _____
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other

DETAILED ACTION

Specification

The specification is objected to for the following reasons.

The specification includes incorrect reference sign "active regions **14**" on page 5, paragraph [0022] of Figure 4. It must be "active regions **34**". Correction is required.

The specification includes incorrect reference signs "contact **18**" on page 6, line 15 and line 17. It must be "contact **38**". Correction is required.

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Background of the Invention in view of U.S. Patent No. 6137128 to Holmes et al.

Regarding to claim 1, Background of the Invention discloses a test circuit comprising a substrate 11; a first deep trench polysilicon layer 12a formed in the

substrate; a first top-thin oxide layer 22a disposed over the first deep trench polysilicon layer 12 a; a second deep trench polysilicon layer 12b laterally formed in the substrate 11 on one side of the first deep trench polysilicon layer 12a; a second top-thin oxide layer 22a disposed over the second deep trench polysilicon layer 12b; a shallow trench isolation 24 embedded in the substrate and located between the first deep trench polysilicon layer 12a and the second deep trench polysilicon layer 12b; an ion well 14c implanted in the substrate and being electrically connected with the first deep trench polysilicon layer; and a contact 18 electrically connecting the ion well 14c and a bit line for supplying the first deep trench polysilicon layer 12a with a pre-selected voltage.

Background of the Invention does not disclose a word line laid on the substrate, the word line partially covering the first top-thin oxide layer, the shallow trench isolation, and the second top-thin oxide layer. Holmes et al. teach a word line laid on the substrate, the word line partially covering the first top-thin oxide layer, the shallow trench isolation, and the second top-thin oxide layer as set forth in col. 9, lines 28-53, and fig. 18.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a word line laid on the substrate, the word line partially covering the first top-thin oxide layer, the shallow trench isolation, and the second top-thin oxide layer, as taught by Holmes et al. in order to increase packing density and to eliminate the problems of conventional memory cell arrays (col. 4, lines 64-65).

Regarding to claim 2, the test circuit wherein the first deep trench polysilicon layer is located at one side of the word line and the second deep trench polysilicon layer is located at the other side of the word line (Holmes: fig. 18).

Regarding to claim 3, the test circuit wherein both of thickness of the first top-thin oxide layer and thickness of the second top-thin oxide layer are smaller than a thickness of the shallow trench isolation (Background of the Invention: figs. 2 and 3).

Regarding to claim 4, the test circuit wherein the shallow trench isolation is formed by performing a shallow trench isolation process (specification, page 2, paragraph [0006].

Regarding to claim 5, the test circuit wherein the first top-thin oxide layer, the second top-thin oxide layer, and the shallow trench isolation are composed of silicon dioxide (spec., page 3, lines 2-3).

Regarding to claim 6, the test circuit wherein the first top-thin oxide layer, the second top-thin oxide layer, and the shallow trench isolation are composed of CVD silicon dioxide (spec., page 3, lines 1-2).

Regarding to claim 7, the test circuit wherein the ion well does not overlap with any word line (figs. 2 and 3).

Regarding to claim 8, the test circuit wherein the word line is composed of polysilicon (figs. 2 and 3).

Claims 9-14 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Background of the Invention in view of U.S. Patent No. 6137128 to Holmes et al.

Regarding to claim 9, Background of the Invention discloses a test key for evaluating isolation quality of a top-thin oxide layer of deep trench DRAM cells, comprising a substrate 11; a first deep trench capacitor 12a formed in the substrate; a first top-thin oxide layer 22a disposed over the first deep trench capacitor 12a; a second deep trench capacitor 12b formed in the substrate 11 and being electrically connected with the first deep trench capacitor 12a; a second top-thin oxide layer 22a disposed over the second deep trench capacitor 12b; a shallow trench isolation 24 embedded in the substrate for isolating the first deep trench capacitor from the second deep trench capacitor; an ion well 14c implanted in the substrate and being electrically connected with the first deep trench capacitor; and a contact 18 electrically connecting the ion well 14c and a bit line for supplying the first deep trench capacitor 12a with a pre-selected

voltage; wherein the second deep trench capacitor is electrically connected with the first deep trench capacitor through a connecting region.

Background of the Invention does not disclose a first word line formed on the substrate partially covering the first top-thin oxide layer, the shallow trench isolation, and the second top-thin oxide layer. Holmes et al. teach a first word line formed on the substrate partially covering the first top-thin oxide layer, the shallow trench isolation, and the second top-thin oxide layer as set forth in col. 9, lines 28-53, and fig. 18.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a first word line formed on the substrate partially covering the first top-thin oxide layer, the shallow trench isolation, and the second top-thin oxide layer, as taught by Holmes et al. in order to increase packing density and to eliminate the problems of conventional memory cell arrays (col. 4, lines 64-65).

Regarding to claim 10, the test key wherein the connecting region comprises a third deep trench capacitor and the shallow trench isolation covers the third deep trench capacitor (Holmes: Figs. 20-21).

Regarding to claim 11, the test key wherein the first deep trench capacitor comprises a polysilicon layer located underneath the first top-thin oxide layer (Background of the Invention: fig. 2-3).

Regarding to claim 12, the test key wherein the polysilicon layer is electrically connected with the ion well through a diffusion region (Background of the Invention: fig. 2-3).

Regarding to claim 13, the test key further comprising a second word line laid on the substrate on at side of the first word line and the second word line partially covers the first top-thin oxide layer, the shallow trench isolation, and the second top-thin oxide layer (Background of the Invention: fig. 2-3).

Regarding to claim 14, the test key wherein the first and second word lines are composed of polysilicon (Background of the Invention: fig. 2-3).

Claim 15 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Background of the Invention in view of U.S. Patent No. 6137128 to Holmes et al.

Background of the Invention discloses a substrate 11; a deep trench capacitor 12a formed in the substrate; at least one active region 14 defined on the substrate, wherein the active region comprises a first region 14a, a second region 14b and an ion well 14c; a thermal oxide layer 15 formed in the first region; a top-thin oxide layer 22a formed in the second region 14b, wherein the second region overlaps with the deep trench capacitor 12a; and at least one word line 16a partially overlapping with the top-thin oxide layer 22a; wherein the ion well 14c is electrically connected with a polysilicon electrode of the

deep trench capacitor and the thermal oxide layer within the first region does not overlap with any word line 16a 16b (Background of the Invention: figs. 2 and 3).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (703) 305-1958. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (703) 308-4910.

The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mai-Huong Tran

HOAI HO
PRIMARY EXAMINER